

FIG. 10 is a schematic diagram of a circuit for measuring the output impedance of a power amplifier.

10

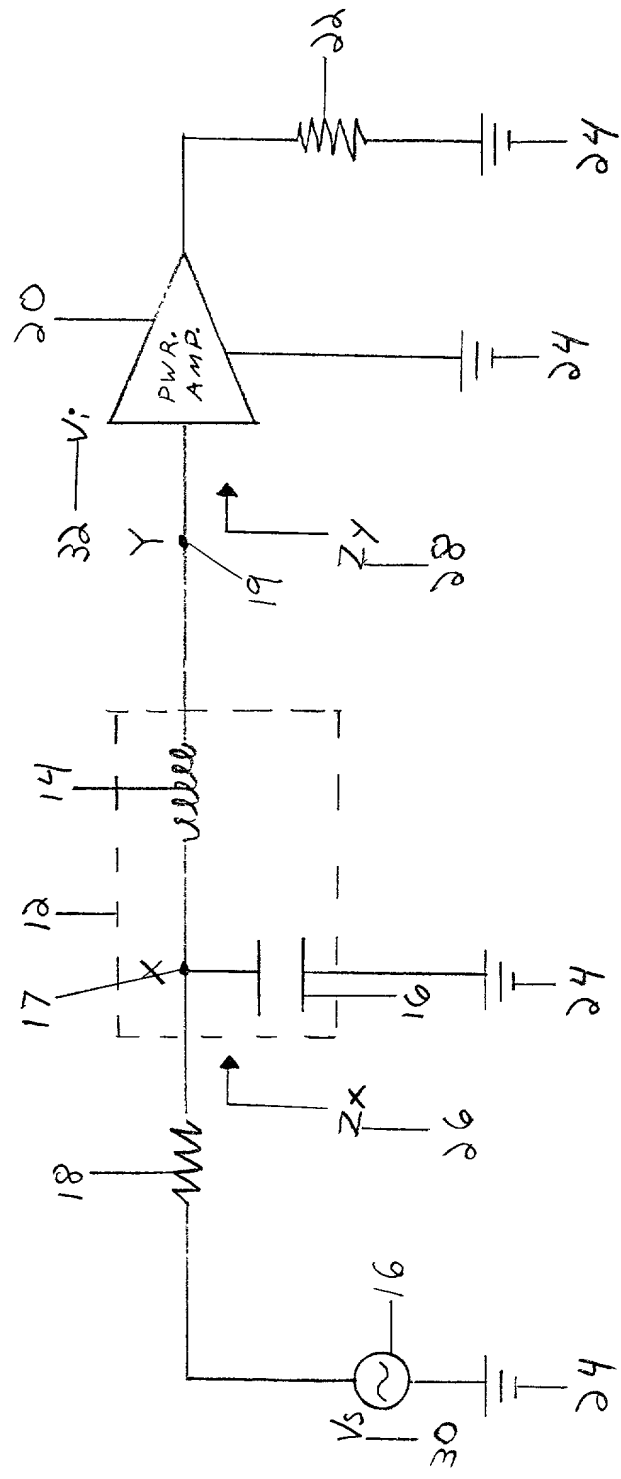


FIG. 1

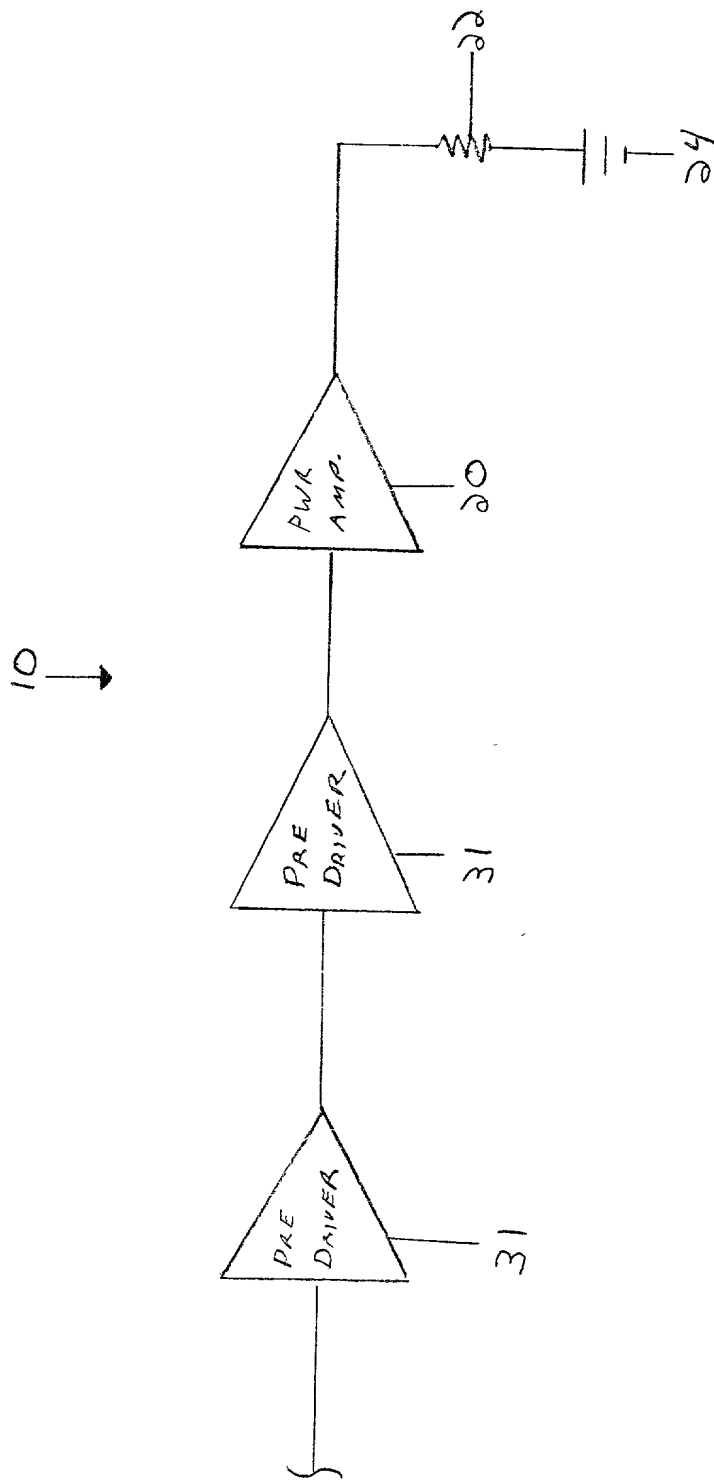


FIG. 2

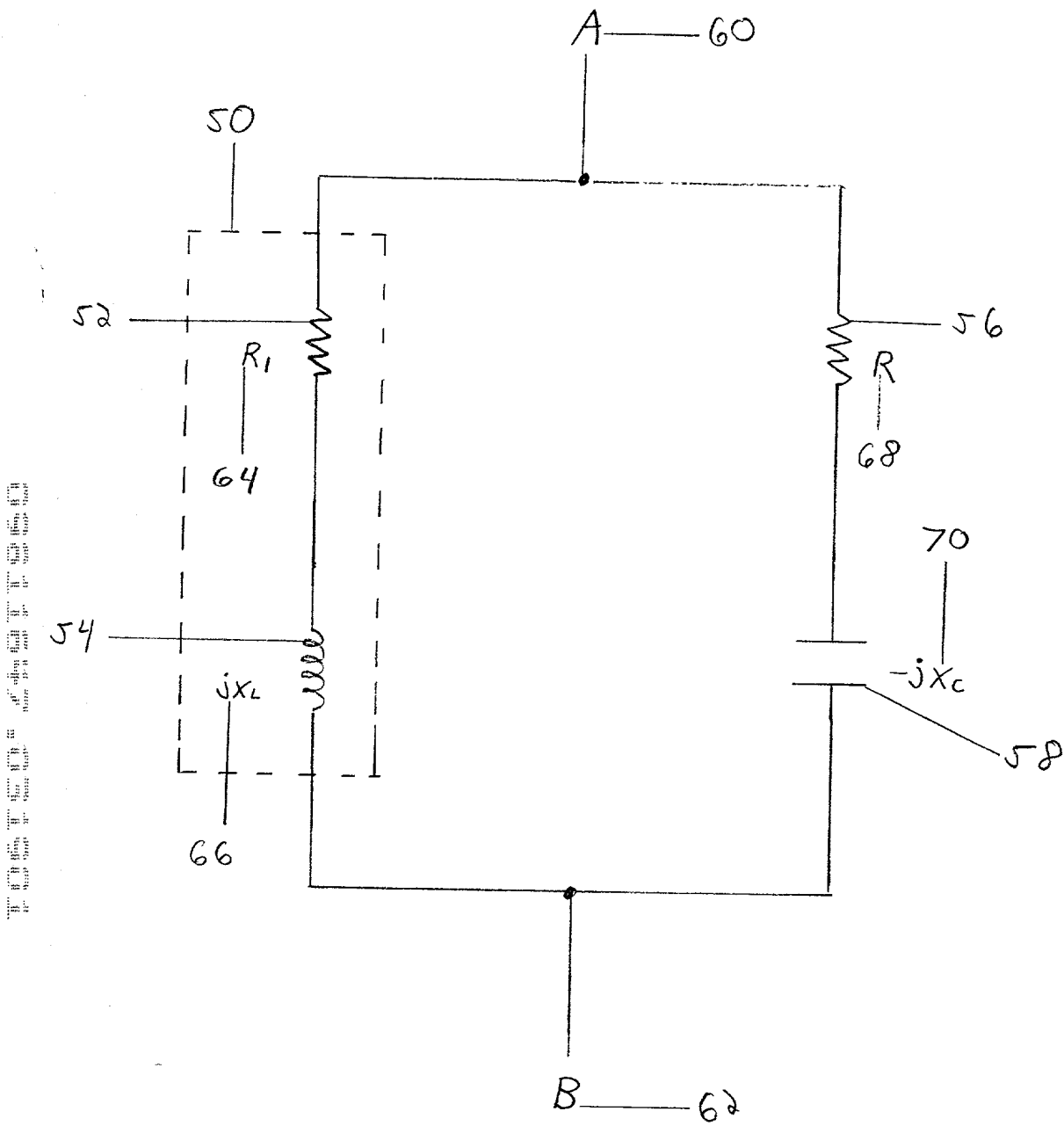


FIG. 3

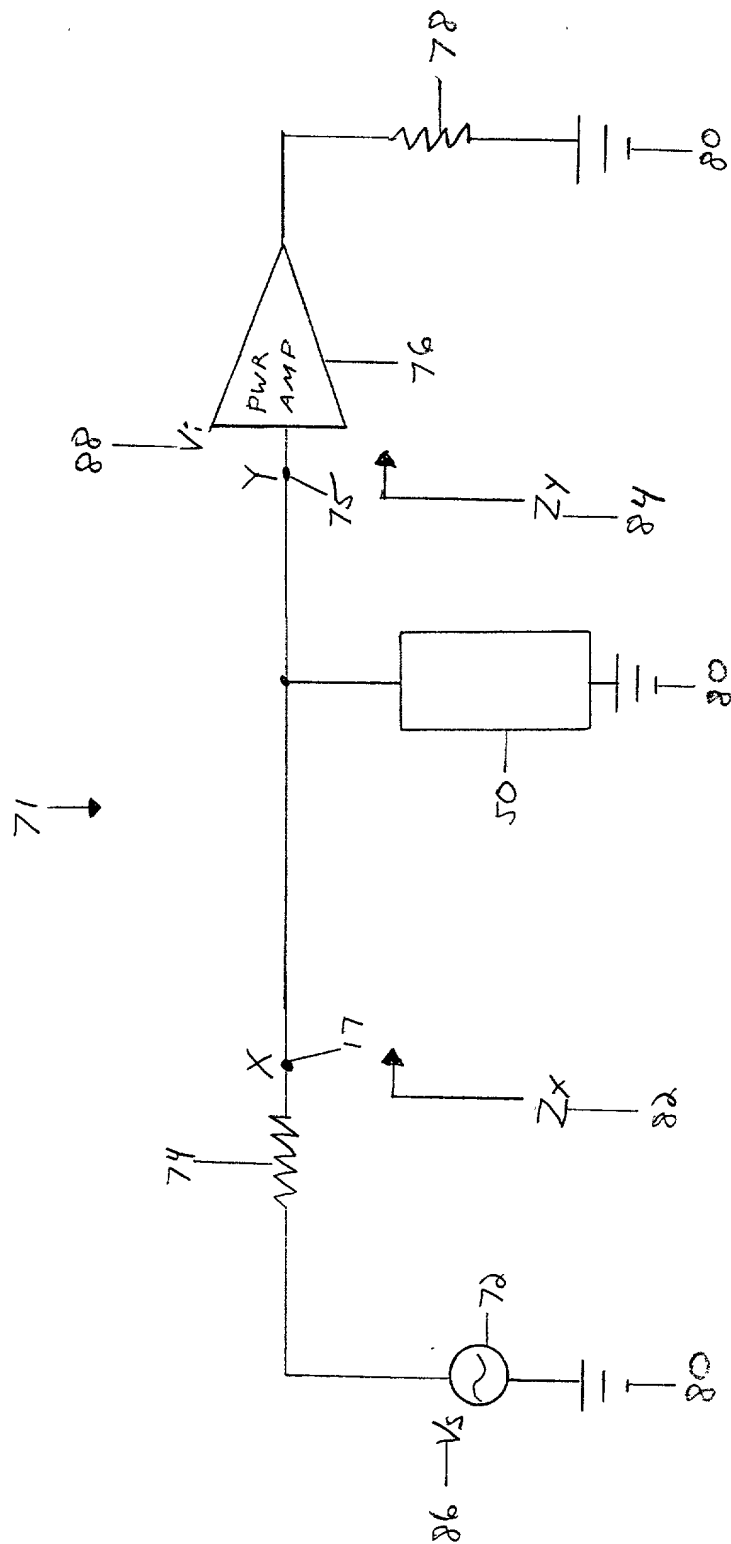


FIG. 4

The following data was obtained from the test of the system.

100

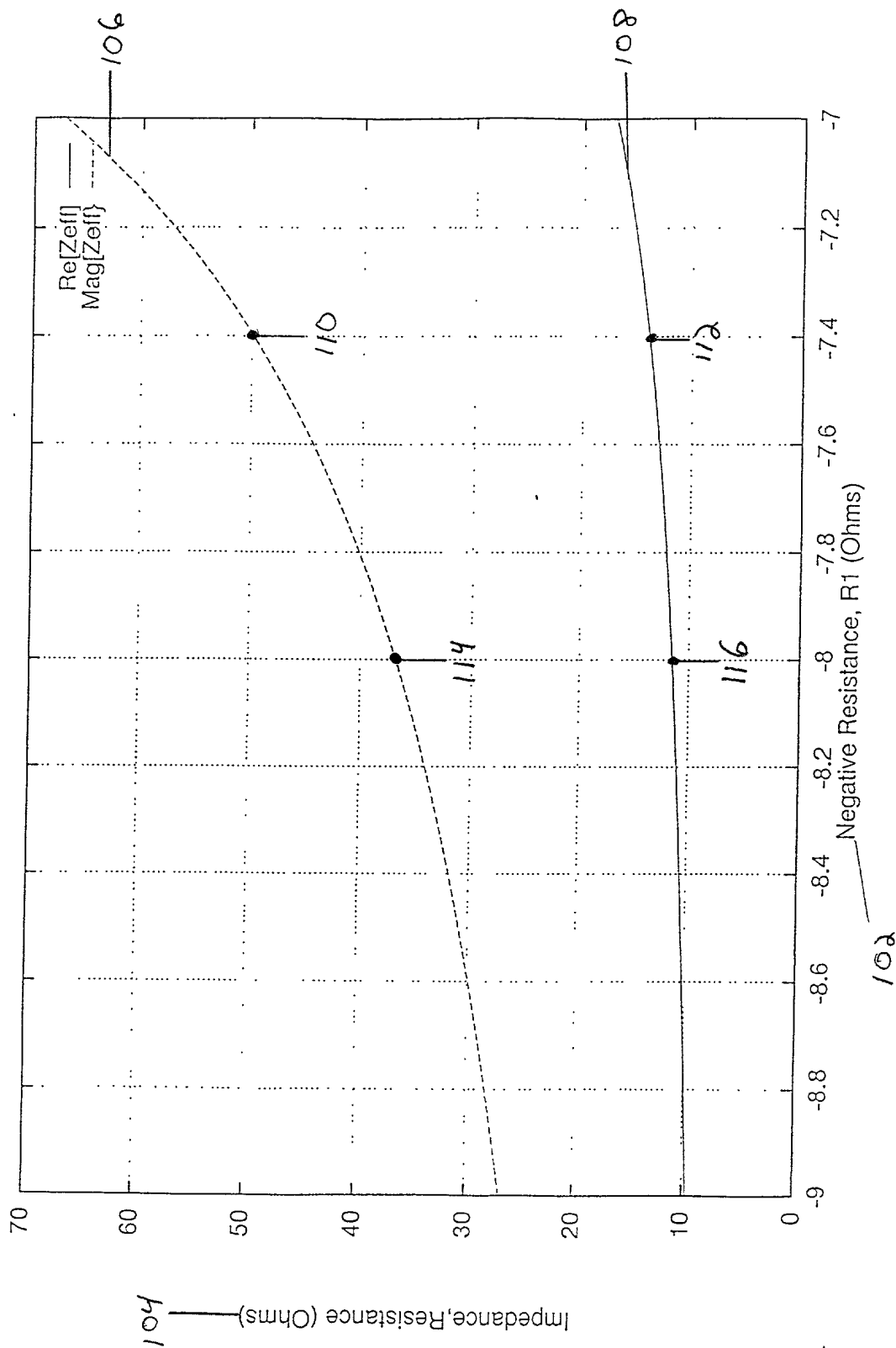


FIG. 5

The following information is provided for the purpose of the present document. It is not intended to be used as a substitute for the original document.

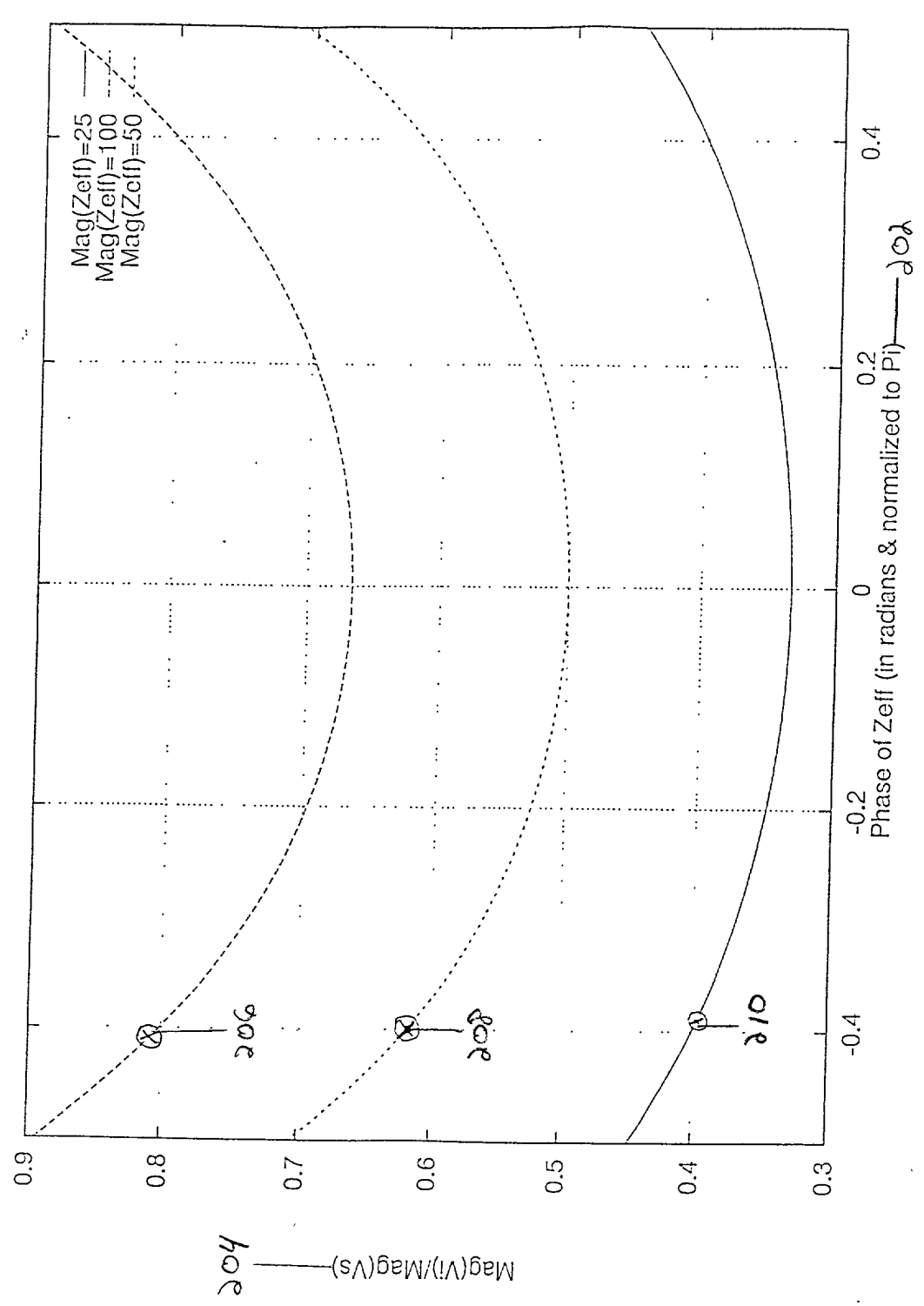


FIG. 6

300

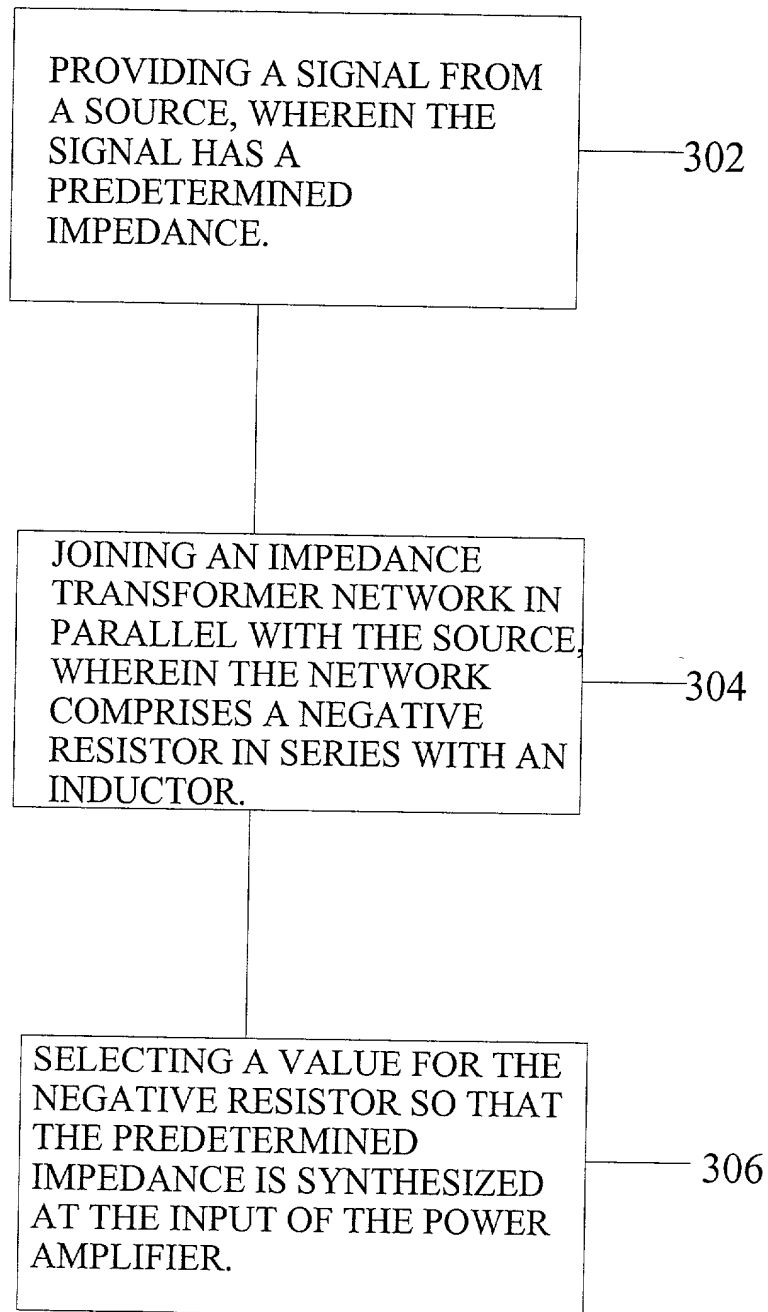


FIG. 7